REMARKS

Claims 2-8, 11-14, and 17-18 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 2-6 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Jones et al (U.S. Pat. No. 6,731,009). This rejection is respectfully traversed.

Claim 2 has been amended and rewritten. More specifically, claim 2 now recites a semiconductor device comprising a rectangle-shaped lower carrier substrate, and an upper carrier substrate mounted on the lower carrier substrate. The lower carrier substrate includes a region without a protruding electrode that is provided along at least two sides which intersect at a first vertex of the upper carrier substrate, and a protruding electrode group which is provided along at least two sides which intersect at a second vertex of the upper carrier substrate opposite the first vertex. Jones et al. does not anticipate such a structure.

More particularly, Jones merely teaches, in Figure 5B, a lower substrate 506 and an upper substrate 508-1. There is no teaching, however, of a semiconductor chip mounted on the upper substrate 508-1. Because this aspect of the claimed invention is not disclosed by Jones, claim 2 is not anticipated.

Claim 3 has also been amended and rewritten. More specifically, claim 3 now recites a semiconductor device comprising a rectangle shaped lower carrier substrate, and an upper carrier substrate mounted on the lower carrier substrate. A

semiconductor chip is mounted on the upper carrier substrate. Lastly, claim 3 recites that the lower carrier substrate includes a region without a protruding electrode which is provided along at least a first side of the upper carrier substrate, and a protruding electrode group which is provided along a second side of the upper carrier substrate opposite the first side, and along at least a third side which intersects a second side. Jones also does not anticipate this structure.

More particularly, Jones fails to disclose a semiconductor chip mounted on the upper carrier substrate. Again referring to Figure 5B of Jones, it can be seen that only a lower substrate 506 with an upper substrate 508-1 disposed thereon is disclosed. There is no disclosure, however, of a semiconductor chip mounted on the upper carrier substrate. Because this aspect of claim 3 is not disclosed by Jones, claim 3 is not anticipated.

Claim 5 has been amended to recite a semiconductor device comprising a lower carrier substrate, and a plurality of upper carrier substrates mounted on the lower carrier substrate. Each of the upper carrier substrates includes a plurality of semiconductor chips stacked thereon. Further, claim 5 recites that a protruding electrode group is arranged on the lower carrier substrate, wherein the protruding electrode group is excluded from a region where a semiconductor chip is mounted on the lower carrier substrate so as to be arranged to be overlapped by ends of the upper carrier substrates. Such a configuration is shown, for example, in Figure 1 of the application.

In Figure 1, it can be seen that a lower carrier substrate 11 includes a plurality of upper carrier substrates 21 and 31 with a plurality of semiconductor chips 24A, 24B, and 24C mounted thereon. Further, a protruding electrode group 26 is arranged on the

lower carrier substrate 11, wherein the protruding electrode group 26 is excluded from a region where a semiconductor chip 13 is mounted on the lower carrier substrate 11 so as to be arranged to be overlapped by ends of the upper carrier substrates 21 and 31. Jones doe not anticipate such a structure.

More specifically, Jones merely discloses a structure wherein a lower substrate 506 includes upper substrates 508-1 and 508-2. Upper substrates 508-1 and 508-2, however, do not support a plurality of semiconductor chips stacked thereon. Because this aspect of the claimed invention is not disclosed by Jones, claim 5 is not anticipated.

Lastly, claim 6 has been amended to recite a semiconductor device comprising a lower carrier substrate, and a plurality of upper carrier substrates mounted on the lower carrier substrate. Each of the upper carrier substrates includes a plurality of semiconductor chips stacked thereon. Claim 6 also recites that a semiconductor chip is mounted on the lower carrier substrate, and a plurality of land electrodes are formed on the lower carrier substrate. A protruding electrode is arranged on each of the plurality of land electrodes. Claim 6 also recites that the upper carrier substrates are supported by the protruding electrodes such that an end of each of the upper carrier substrates overlap the semiconductor chip mounted on the lower carrier substrate. Again, such a configuration is supported in the present application in Figure 1.

More specifically, a lower carrier substrate 11 includes a plurality of upper carrier substrates 21 and 31 mounted thereon. Each of the upper carrier substrates 21 and 31 include a plurality of semiconductor chips 24A, 24B, and 24C stacked thereon. Lastly, Figure 1 depicts that a semiconductor chip 13 is mounted on the lower carrier substrate, and a plurality of land electrodes 12C are also formed on the lower carrier substrate. A

protruding electrode 26 and 36 is arranged on each of the plurality of land electrodes 12C, wherein the upper carrier substrates are supported by the protruding electrodes 26 and 36 such that an end of the upper carrier substrates 21 and 31 overlap the semiconductor chip 13 mounted on the lower carrier substrate 11.

Jones does not anticipate such a structure. Jones, again as stated above, merely discloses a lower substrate 506 including upper substrates 508-1 and 508-2 mounted thereon. These upper carrier substrates, however, do not support a plurality of semiconductor chips stacked, as claimed. Because this aspect of the claimed invention is not disclosed Jones, claim 6 is not anticipated.

Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

NEW CLAIMS

New claims 17 and 18 have been added. New claims 17 and 18 recite semiconductor devices according to claims 2 and 3, respectively, further comprising a plurality of upper carrier substrates mounted on the lower carrier substrate. New claims 17 and 18 also recite that a plurality of semiconductor chips are stacked on each of the upper carrier substrates. As stated above, under the rejection under 35 U.S.C. § 102(e), Jones does not anticipate such a structure. Accordingly, Applicant respectfully asserts that new claims 17 and 18 are in condition for allowance.

ALLOWABLE SUBJECT MATTER

Applicants acknowledge, with thanks, the allowance of claims 7, 8, and 11-14.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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